PhD Project

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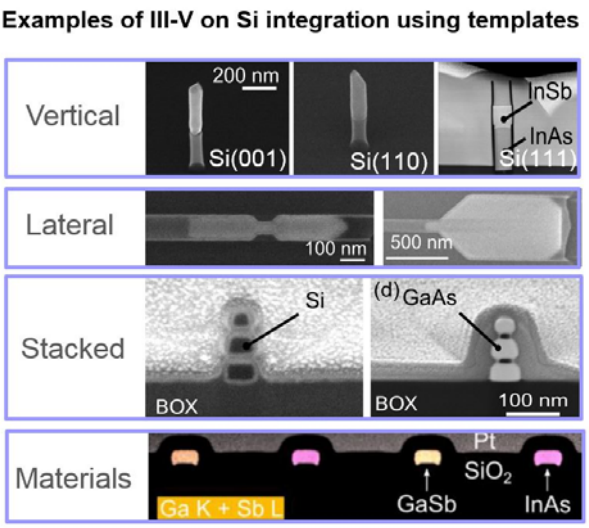
Title:
Alternative semiconductor materials and architectures for nanoelectronic devices



Introduction:
Recent developments of microelectronic technologies make increasing use of alternative semiconductors of the IV-IV and III-V groups, alternative high-k and low-k dielectrics and new device architectures (e.g. FinFET, stacked nanosheets and nanowire, etc.) to yield improved device performance at the ultimate scaling limits. In a longer term perspective, two-dimensional materials are also showing promising properties. In addition, besides mainstream CMOS, integrated optoelectronics and quantum computing take advantage of co-integration onto Silicon (e.g. via wafer bonding or local epitaxial growth techniques). Unfortunately, noise, native and generated defects and fluctuation phenomena hamper the performance of new devices in these advanced technologies (especially when dimensions are tiny). Any credible performance assessment study should carefully consider all these factors at both the device and circuit level.

Proposed research activity and PhD thesis objectives:
The objective of the PhD thesis is to investigate the noise generation mechanisms and the fluctuation sources in the semiconductor (channel) and insulators (gate dielectric and passivation layers) of advanced devices fabricated in MOSFETs and APD structures with alternative III-V semiconductor and 2D material channels for switching and sensing applications.
Advanced simulation tools, ad hoc models and commercial TCAD will be used to investigate nominal device performance and benchmark the results to standard CMOS components. Variability, noise and fluctuation sources (considered in their discrete characteristics) will be included in the analysis. Compact models based on lumped elements and Verilog-A codes will be developed to enable circuit- and mixed-mode device-circuit simulations of elementary analog and digital blocks realized with these new technologies. Comparison to experimental data provided by international partners will be part of the activity.

Vision goals of the activity: The ultimate goals of the study are: 1) to develop simulation models calibrated on measurements, to predict the performance and variability of advanced devices for More Moore and More than Moore applications fabricated at partner institutions; 2) to investigate the attractiveness of these new technologies up to the level of elementary analog and digital circuit blocks; 3) to provide compact models suitable to carry out circuit designs.

Supporting research projects (and Department)
The activity will be carried out at the DIEF, Università degli Studi di Modena e Reggio Emilia and may include a stage at a partner institution in Europe

Possible connections with research groups, companies, universities.
Tyndall national institute, University College Cork (Ireland)
University of Lund
IUNET Research Consortium (www.iunet.info)